WHAT IS CLAIMED IS:

1. An image processing system adapted to process image frames and comprising:

an image processing engine adapted to perform object-independent processing corresponding to a first layer of the image processing system, said image processing engine further adapted to include a plurality of processors each associated with a different one of pixels of the image frame;

a post processing engine adapted to perform object-dependent processing corresponding to a second processing layer of the image processing system, said post processing engine further adapted to include an N-way symmetric multi-processing system (SMP) having disposed therein N DFT engines and N matrix multiplication engines; wherein N is an integer greater than 1, and

a processing engine adapted to perform object composition, recognition and association corresponding to a third processing layer of the image processing system.

2. The image processing system of claim 1 wherein the plurality of processors of the image processing engine form a massively parallel processing system.

3. The image processing system of claim 2 wherein the massively parallel processing system is a systolic array type massively parallel processing system.

4. The image processing system of claim 3 wherein the systolic array type massively parallel processing system is configured as a single-instruction multiple-data system.

5. The image processing system of claim 1 wherein each of the plurality of the processors is further adapted to perform a unified and symmetric processing of N dimensions in space and one dimension in time.

6. The image processing system of claim 1 further comprising:

an image capturing block.

7. The image processing system of claim 6 wherein the plurality of processors are formed on a first semiconductor substrate different from a second semiconductor substrate on which the image capturing block is formed.

8. The image processing system of claim 7 further comprising:

a realignment buffer adapted to realign the data received from first and second analog-to-digital converters disposed in the image capturing block.

9. A method for processing images:

performing object-independent processing corresponding to a first image processing layer;

performing object-dependent processing corresponding to a second processing layer and using an N-way symmetric multi-processing system (SMP) having disposed therein N DFT engines and N matrix multiplication engines; wherein N is an integer greater than 1; and

performing object composition, recognition and association corresponding to a third processing layer.

10. The method of claim 9 further comprising:

performing object independent processing by a plurality of processors that form a massively parallel processing system.

11. The method of claim 10 wherein the massively parallel processing system is a systolic array type massively parallel processing system.

12. The method of claim 11 further comprising:

configuring the systolic array massively parallel processing system as a single-instruction multiple-data system.

13. The method of claim 12 wherein each of the plurality of the processors is further adapted to perform a unified and symmetric processing of N dimensions in space and one dimension in time.

14. The method of claim 13 further comprising:

capturing the image frame on a first semiconductor substrate that is different from a second semiconductor substrate on which the plurality of processors are formed.

15. The method of claim 14 further comprising

converting analog data corresponding to the image frame to digital data; and

realigning the converted digital data.